

Fifth Semester B.E. Degree Examination, December 2010
Fundamentals of CMOS VLSI

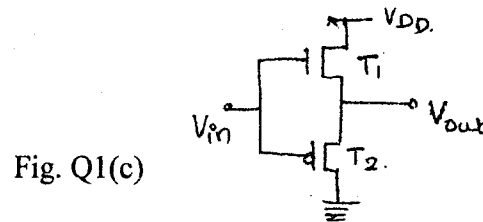
Time: 3 hrs.

Max. Marks:100

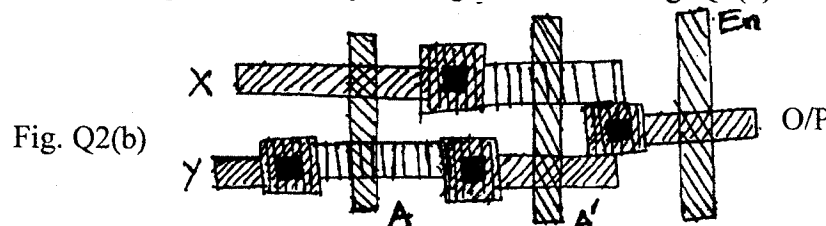
Note:1. Answer any FIVE full questions, selecting atleast TWO questions from each of Part – A and Part - B.
2. Missing data may be assumed suitably.

PART – A

- 1 a. What do you mean by static load inverters? Derive the output voltage for the pseudo inverter by discussing its DC transfer characteristics. (08 Marks)
- b. In a $0.5\mu\text{m}$ process $\mu_n = 44.69 \times 10^{-3} \text{ m}^2/\text{V}$, $t_{\text{ox}} = 14.1\text{nm}$ and the $(W/L) = \frac{30}{5}$. The NMOS has $V_t = 0.71\text{V}$ and $V_{\text{gs}} = 1.5\text{V}$. At what levels of V_{ds} and i_d , will the MOSFET reach pinch off mode? Hint : $(\epsilon_{\text{ox}} = 3.9\epsilon_0)$. (06 Marks)
- c. What is the functionality of the circuit shown in fig. Q1(c). Is it correct method to connect the circuit as shown in figure Q1(c)? Justify your answer. (06 Marks)



- 2 a. Draw the Cmos circuit for half adder. (Hint : Sum = $A \oplus B$, carry = AB , Inverted i/p^s are allowed). (08 Marks)
- b. Draw the circuit diagram for the layout diagram shown in fig. Q2(b). (08 Marks)



- c. What are the basic layers of MOS circuit? (04 Marks)
- 3 a. Explain the working principle of dynamic CMOS logic and clocked CMOS logic of "Nand" gate. (12 Marks)
- b. Implement the pass transistor logic circuit for the expression $Y = A + BC$. Show the design steps clearly. (08 Marks)
- 4 a. Discuss the limitations of scaling. (10 Marks)
- b. Derive the expression for total delay for N stage of NMOS and CMOS inverters by assuming the width factor $f = e$. (10 Marks)

PART - B

- 5 a. In the circuit shown in fig. Q5(a), find V_1 , V_2 , V_3 , V_4 and V_5 . Justify your answer. (08 Marks)

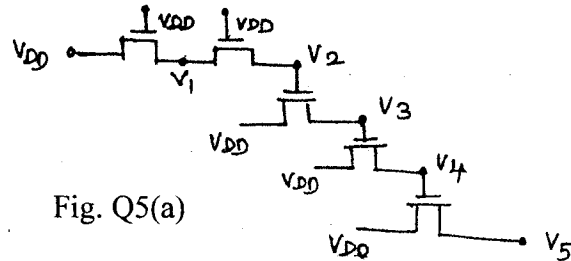


Fig. Q5(a)

- b. Explain NMOS and CMOS non – inverting dynamic storage cell and draw the 3 – bit shift register using the CMOS dynamic storage cell. (12 Marks)
- 6 a. Draw and explain the 8 – bit carry select adder dividing it into $m = 2$ blocks. Calculate the completion time ‘T’ by assuming the one adder delay is 4ns and one mux delay is 2ns. (12 Marks)
- b. Draw the block diagram and clearly show the switch connections to perform the logic operation of “OR” and “XOR” in a 3 – bit ALU using a standard adder element. (08 Marks)
- 7 a. Explain four transistor dynamic and six transistor static memory cells. Reason out the need for sense amplifier in the cell array. (14 Marks)
- b. Explain the CMOS pseudo – static D flipflop. (06 Marks)
- 8 a. What is multiplexed D flipflop? Explain the general method for testing with scan path approach. (08 Marks)
- b. What are the three important steps in sensitized path based testing? (06 Marks)
- c. Find the test vectors to detect the stuck @ 0 and stuck @1 faults of “and” gate at its input and output node. Fig. 8(c). (06 Marks)

Fig. Q8(c)

